MB86961A

UNIVERSAL INTERFACE FOR 10BASE-T

Application Note: CONNECTING TO THE MC68EN360 QUICC March 1997

Overview

This application note describes one method of connecting the Fujitsu MB86961A Universal Interface for 10Base-T to the Motorola MC68EN360 Quad Integrated Interface Controller (QUICC) which has specially designed Ethernet capability. The MB86961A meets all of the design requirements of the Motorola QUICC with a minimum of external circuitry.

The circuit connections are shown in Figure 1. Care should be taken in the layout to isolate the bias current by locating the resistor close to the pin. If this resistor is not positioned properly it may act as an antenna and cause erratic performance. Ensure that this bias resistor is placed away from other components as well as signal traces and do not run any signals under it. Also ensure to use a bypass capacitor at each Vcc pin.

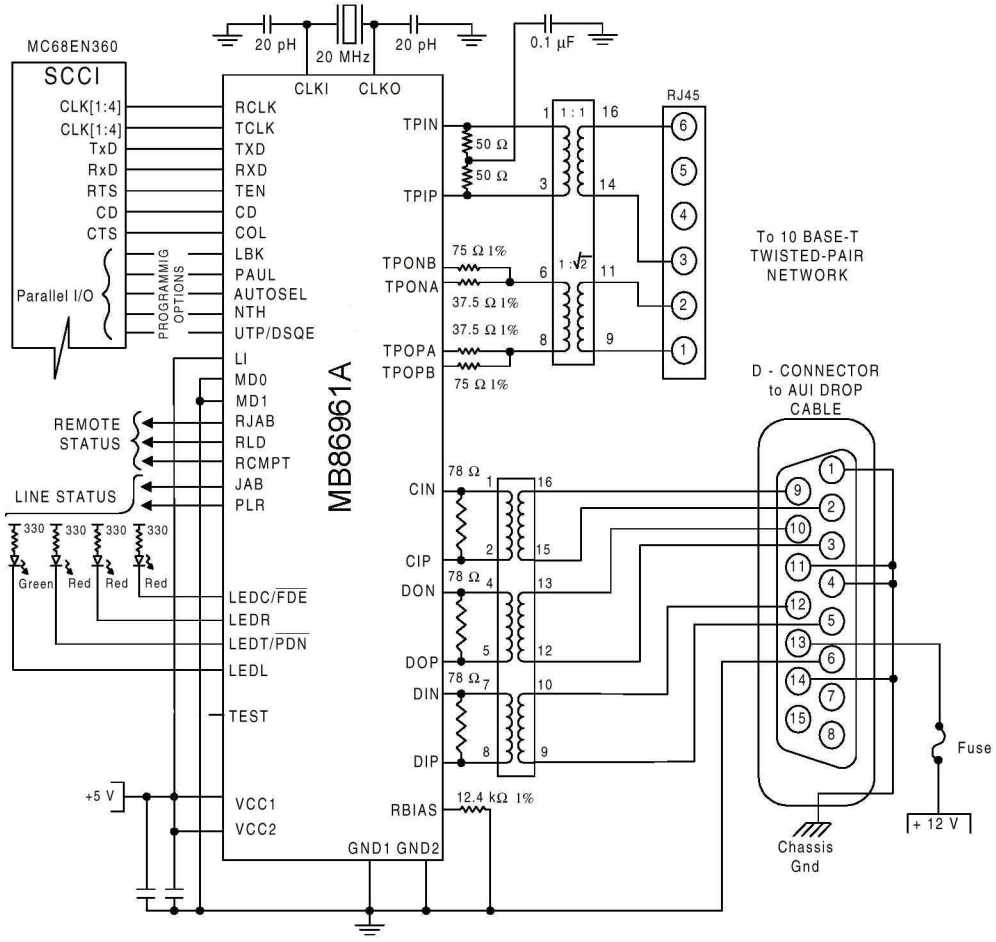

Figure 1: Interface Between the MB86961A and the MC68EN360

MB86961A to QUICC Interface

The MB86961A is available in either a 44-pin PLCC or a 48 pin PQFP. The following pins on the MB86961A connect to the MC86EN360 signals as shown in Table 1.

MB86961A Device			MC86EN360 SCC1 Signal
PLCC	PQFP	Signal	
28	36	RCLK	CLK1-4[1]
11	17	TCLK	CLK1-4[1]
12	18	TXD	TXD
26	34	RXD	RXD
13	20	TEN	RTS[2]
27	35	CD	CD[2]
16	23	COL	CTS[2]
22	29	LBK	Connect these bits to the Parallel I/O bus on the QUICC[3] and program as needed.
40	1	PAUI	
17	24	AUTOSEL	
4	10	NTH	
37	46	UTP	

Notes:
1. The design must provide separate clocks for TCLK and RCLK. Any of the clocks on the QUICC may be used.
2. These signals are active high in this application.
3. Check with the MC86EN360 Users Manual for the specific connections needed.

Table 1: Pin Connections Between the MB86961A and the MC68EN360

External Components

The design shown in Figure 1 requires two DIP transformer packages for isolation and impedance matching on the AUI or twisted pair transmit and receive lines. The recommended transformers and the list of components for the design are shown in Tables 2 & 3.

Manufacturer	Part Number	TP/AIU
Bel Fuse	S553-0716/A553-0716	TP
	A553-0756/S553-0756	AUI
Fil-Mag	23Z128/23Z128	TP
	23Z90/23Z90SM	AUI
HALO Electronics	TD42-2006Q	TP
	TG42-2006WH1	
	TD01-0756K	AUI
	TD01-0756W	
Valor	PT4069/SM4069	TP
	LT6030/SM6030	AUI

Component	Qty
37.5 Ω, 1%	2
50 Ω, 1%	2
75 Ω, 1%	2
78 Ω, 1%	3
300 Ω, 1%	4
12.4 kΩ, 1%	1
18 pF	1
20 pF	2
0.1 uF	3
20 MHz Xtal	1
Green LED	1
Red LED	3

Tables 2 & 3: Transformers and Components for Ethernet Design

Setting the QUICC Parameters

Refer to the MC68360 Users Manual for settings required to insure proper functionality. Please note the following:

- The only communication port which has Ethernet functionality is SCC1. Use SCC1 for the LAN connection and another SCC (or a parallel) port for the other side of the connection.
- Bypass both the Digital Phase-Locked Loop (DPLL) and Manchester Encoding/Decoding function for Ethernet operation.
- The TCI (Time Clock Invert) bit must be High to allow the QUICC to clock the data out to the MB86961A on the rising edge of the clock pulse. This improves data setup time at the 10 Mbps speed used by Ethernet. TCI is bit 28 of the General SCC Mode Register (GSMR).
- The Mode bits (0-3) must be set to 1, 1, 0, 0 respectively. The Transparent Receiver (TRX) and Transparent Transmitter bits (TTX), bits 43 and 44, must both be 0 (normal operation) or 1 (transparent operation). Do not mix TRX and TTX values. The 0 setting is recommended; in transparent mode, the QUICC does not manipulate protocols in the data stream.
- The transmit FIFO Length (TFL) bit should be 0. TFL is bit 38 is the GSMR. The Receive FIFO Width (RFW) bit, bit 37, should also be 0.
- GSMR bits 19 and 20 are the Transmit Preamble Pattern (TPP) bits. For Ethernet operation, set them to 0, 1 to transmit a repeating 10 pattern as a preamble.